

# LDMOS ELECTRO-THERMAL MODEL VALIDATION FROM LARGE-SIGNAL TIME-DOMAIN MEASUREMENTS

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**Abstract** — Analytical non-linear model validation through large-signal time-domain characterization has been greatly improved, by establishing a novel link between measurement and simulation. Investigation on a Silicon LDMOS device and its non-linear electro-thermal model positively identifies links between model formulation and amplifier requirements for future telecommunication systems.

## I. INTRODUCTION

A key requirement for a reliable use of CAD tools in radio-frequency power amplifier design is the accurate extraction and validation of transistor non-linear models. Traditional techniques for device model extraction are DC or pulsed I-V's and s-parameters, while the model is eventually utilized for prediction of large-signal operation. Typical model validation procedures are developed focusing on particular amplifier design aspects such as power, efficiency and linearity. Usually this involves the selection of a measurement environment, e.g. through a load-pull system [1], or even the design of a test circuit to be measured [2]. In all cases accurate reproduction of the modeled device measurement environment within the CAD simulation can be critical for a correct model validation. This problem is complicated by the use of diverse characterization techniques, making data interpretation difficult and introducing the potential for misleading results. Recently non-linear vector network analyzer (NVNA) systems, integrated with harmonic load-pull, have emerged as suitable tools for transistor characterization and non-linear large-signal modeling [3, 4]. In this work it will be demonstrated how large-signal time-domain characterization performed with a NVNA provides for the ideal non-linear model validation. A direct use of measured large-signal time-domain waveforms within Harmonic Balance simulation is utilized which eliminates issues in describing the device measurement environment and allows for model parameter optimization. Results on a Silicon LDMOS device for RF applications and its electro-thermal model are presented. Amplifier operation specific issues such as

power and linearity are addressed during model validation, directly analyzing the dynamic large-signal behavior. Through direct access of the model internal branch currents possible weaknesses of the model formulation are also identified.

## II. HARMONIC BALANCE SIMULATION FROM LARGE-SIGNAL TIME-DOMAIN DATA

Traditional large-signal Harmonic Balance simulation for model validation involves a complete description of the device measurement environment, such as bias networks, source and load reflection coefficients, source power, etc. A simpler alternative is available when large-signal time-domain data is obtained from a NVNA measurement. Figure 1 shows the proposed simulation test-bench based on the use of input and output measured voltage waveforms as stimuli for the non-linear model (shaded box). The resulting simulated input and output current waveforms are available for comparison to the measured currents, for model validation purposes. Any commercial simulator will allow this setup. Both Agilent ADS1.3 and Aplac simulators are used in this work, depending on the particular application.

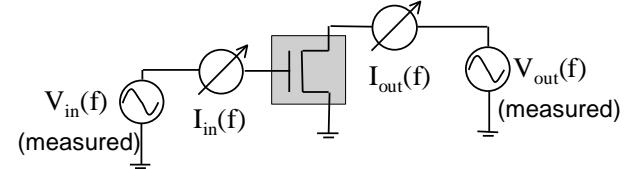


Fig. 1. Schematic of the Harmonic Balance simulation from time-domain large-signal data.

This voltage stimuli based simulation investigates the model behavior by probing directly its effective voltage controlled current response. Any interaction between terminal voltages and currents through the source and load impedances is avoided. Therefore difference between simulated and measured large-signal behavior can be linked directly to current contributions of the model constituent parts. This will prove most advantageous in the

following model validation discussion. Furthermore an accurate model will automatically reproduce the complete device measurement environment information.

### III. MODEL EXTRACTION AND VALIDATION

The devices used in this study are part of the 4<sup>th</sup> generation LDMOS transistors from Motorola [5]. The transistor has 12 gate fingers, 200 $\mu$ m unit gate width, 0.6 $\mu$ m gate length and 2.4mm of total gate periphery. Ground-signal-ground pads are included for on chip testing. The utilized device large-signal model was presented in [6]. It is an empirical function based electro-thermal model, which includes dynamic self-heating effects.

The model parameters describing the real drain-source current generator, breakdown current and the thermal coefficients have been extracted from pulsed (isothermal) and DC I-V measurements at different heat-sink temperatures, in order to de-couple thermal and electrical model dependencies. The non-linear capacitance functions have been fitted to extraction results from small-signal off-state measurements [7]. The model also includes a gate transit time delay, which is directly extracted from large signal current and voltage waveforms measured into a short circuit fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics load, the details not being covered here for brevity.

In order to evaluate the accuracy of the extracted model in predicting large-signal waveforms at 2GHz, a set of measurements was chosen for maximum coverage of the state-variables plane ( $V_{GS}, V_{DS}$ ) [4]. For this purpose a high reflection coefficient load obtained by a short circuit connected through a phase shifter was sufficient. By rotating the phase of the load around the smith-chart, a set of rotating dynamic load-lines was achieved as shown in Fig. 2. The model is able to predict all the major features

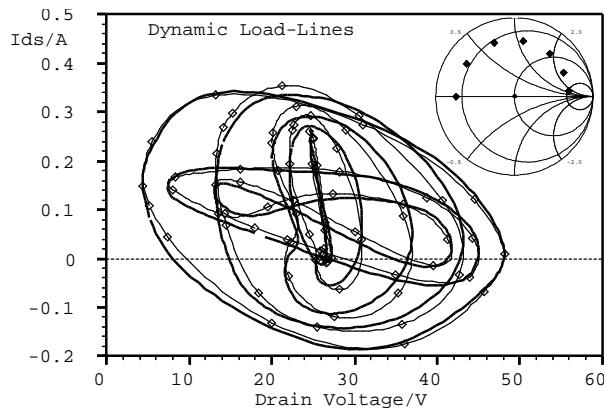


Fig. 2. Measured (markers) and simulated (solid lines) dynamic load-lines at 2GHz fundamental, using the rotating phase fundamental loads shown in inset.

in the waveforms while showing some limitations. Therefore the feasibility of optimization of the model directly from large-signal data was investigated, by using the same measurement strategy for maximum output plane coverage. Defining the error function for optimization in the frequency domain has proven to be simpler and more robust. Each significant harmonic component of gate and drain large-signal currents gives an error function term:

$$\epsilon_k = \log(\max(|\bar{m}_{l,k} - \bar{s}_{l,k}|, 10^{-20})) + 20 \quad l = \text{gate, drain} \quad (1)$$

where  $k$  is the overall harmonic index for the complete measurement,  $m$  and  $s$  are the measured and simulated current harmonic vector components respectively. The logarithm and  $\max$  functions account for orders of magnitude differences between significant current harmonics, while ensuring the correct weighting between the harmonic terms. The overall error function to be minimized during parameter optimization will be the  $p$ -norm summation defined as:

$$E = \left[ \sum_{k=1}^K (\epsilon_k^p)^{\frac{1}{p}} \right] \quad (2)$$

where  $p$  is usually set to 2. Although this optimization technique has proven to attain convergence, no significant improvements from results shown in Fig. 2 could be achieved.

### IV. LARGE-SIGNAL AMPLIFIER OPERATION

In order to identify the implications of model limitations on large-signal amplifier performance, the device has been investigated tuned for class AB power amplifier operation. A power sweep measurement has been performed using the NVNA with a fundamental frequency load chosen for maximum power. The resulting large-signal data was utilized for simulation and non-linear model investigation. Figure 3 shows the measured and simulated dynamic load-lines, labeled with the corresponding power gain, on top of pulsed I-V traces included for reference. The top half of the graph shows also the model drain capacitance function versus drain voltage. It is worth noting that the dynamic voltage waves enter the non-linear capacitance region already at relatively low compression levels, indicating the relevance of this non-linearity to the compression mechanisms.

The power performances of the device can be analyzed from the same data by taking the scalar powers of the signal harmonic components. Figure 4 contains the output power at the fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonics, and the power gain, versus input power. Only a small discrepancy between measured and predicted gain compression is

observed, while the harmonic content is well behaved. This traditional scalar information addresses the power performances but is also usually associated to magnitude related distortion mechanisms of the device (AM/AM). It does not account though for the clear differences between measured and simulated compressed waveforms, which will be related to phase distortion mechanisms (AM/PM).

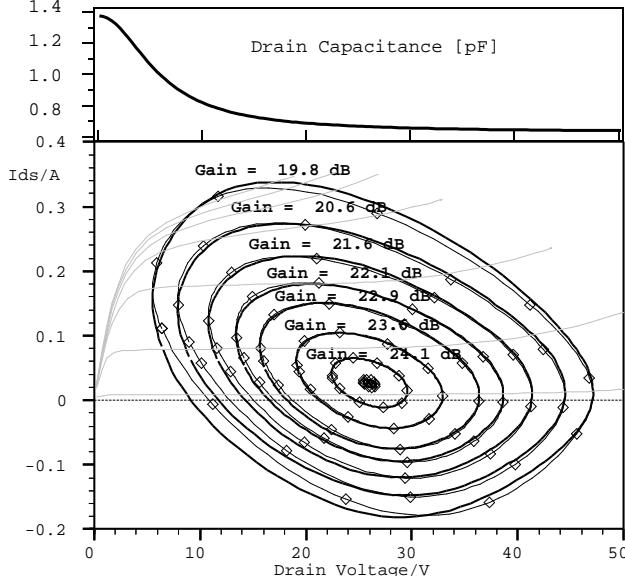


Fig. 3. Bottom: measured (markers) and simulated (solid lines) dynamic load-lines for class AB operation (pulsed I-V traces in the background). Top: drain capacitance function.

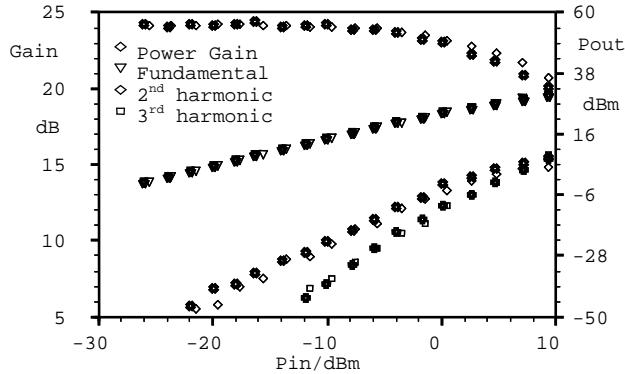


Fig. 4. Measured (thin markers) and simulated (thick markers) scalar output powers at the first three harmonics and power gain from the class AB measurement data.

In order to provide for a model validation tool in this respect, a quantitative formulation of magnitude and phase large-signal data from the waveforms must be utilized. Solutions to the general problem of describing non-linear systems in the frequency domain have been recently proposed, such as the Volterra series based "VIOMAP" model [8] or the use of "describing functions" [9]. For the

present discussion on our large signal data, a simpler quantity, which relates a certain output wave harmonic component to the single sinusoidal input wave will be introduced. A "wave harmonic ratio", which will be referred to as  $R_{ij}(k)$ , can be defined as:

$$R_{ij}(k) = \frac{b_i(k \cdot f_0)}{a_j(f_0)} \quad i, j = 1, 2 \quad k = 1..K \quad (3)$$

Where  $a$  and  $b$  are the incoming and outgoing travelling waves respectively,  $f_0$  is the fundamental frequency,  $k$  is one of the significant harmonic components,  $i$  and  $j$  are the port indexes of the two-port which describes the device. This definition, which could also be related to the harmonic components of the large-signal s-parameters, will give complex quantities that can be plotted in a polar plot or on a smith-chart, while increasing the power level. Figure 5 shows the forward transmission ratio  $R_{21}$  at fundamental, 2<sup>nd</sup> and 3<sup>rd</sup> harmonic, together with the fundamental input reflection coefficient  $R_{11}$ , plotted for the same power sweep levels of Fig. 4.

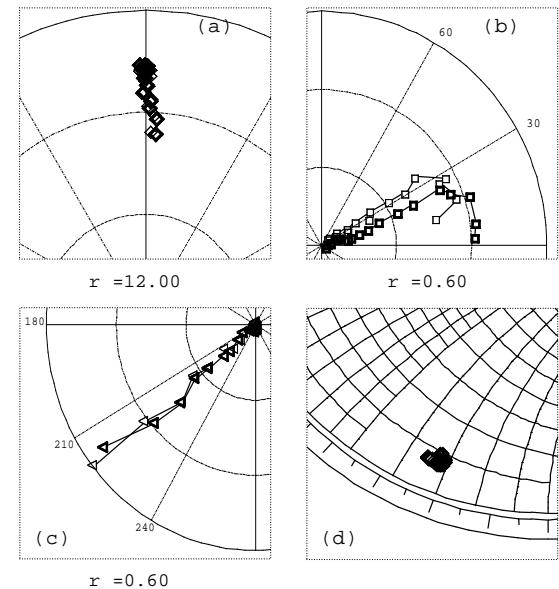


Fig. 5. Measured (thin markers) and simulated (thick markers) transmission ratio at fundamental  $R_{21}(1)$  (a), second  $R_{21}(2)$  (b) and third  $R_{21}(3)$  (c) harmonic, and input reflection ratio at fundamental  $R_{11}(1)$  (d), at increasing input power.

The level of model accuracy in predicting both magnitude and phase of these parameters up to the third harmonic can be observed. Figure 5 also shows some issues as the device enters compression, which relate to the slight measured/simulated current deviations within compressed load-lines in Fig. 3. These might have implications on the model capability of predicting AM/AM and AM/PM distortion in saturation.

## V. LARGE-SIGNAL MODEL DIAGNOSIS

Once the non-linear model behavior under large-signal operation has been analyzed, further steps can be taken in investigating probable causes of identified problems. Compression related issues emerging from previous discussion can be attributed to drain current prediction accuracy issues at increasing power level (see Fig. 3), especially when the drain voltage sweeps into the non-linear region of  $C_{DS}$ . An attempt is therefore made to identify the cause of the problem by analyzing the internal branch large-signal currents of the model separately, plotted versus the control gate voltage (see Fig. 4 in [6] for model schematic).

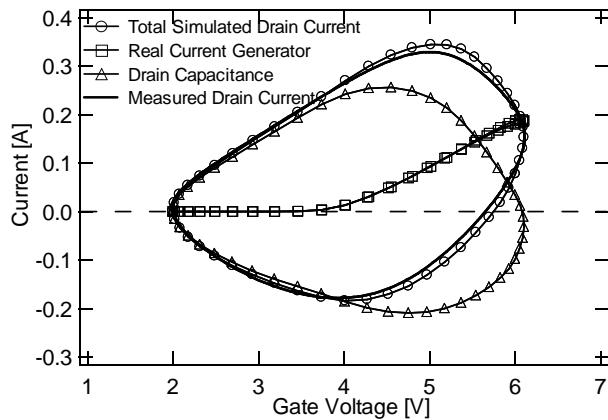


Fig. 6. Simulated total drain current with its real and displacement components, compared to the measured.

From the results in Fig. 6 an excessive displacement current within the total simulated drain current (circles) compared to the measured (solid lines) can be clearly related to the higher gate voltage values. The model non-linear  $C_{DS}$ , only a function of the drain voltage, is identified as the probable source of the problem, indicating the necessity to introduce some gate-voltage dependence for more accurate prediction of gain compression mechanisms [3].

## VI. CONCLUSION

A novel and most comprehensive use of large-signal time-domain characterization for non-linear model validation has been extensively investigated. A novel Harmonic Balance simulation test-bench based on direct input and output measured large-signal time-domain voltage waveforms as stimuli for the non-linear model proved advantageous. Any issue on describing the device measurement environment was eliminated and model parameter optimization was attainable. The analysis of the dynamic large-signal behavior of a Silicon LDMOS

device and its electro-thermal model, focused on amplifier operation specific issues such as power and linearity, gave a comprehensive model validation. Furthermore, probable weaknesses of the model formulation were positively identified through the analysis of model internal branch currents.

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